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Real Time On Chip Implementation Of Dynamical Systems With

Abstract Simulation of large-scale networks of spiking neurons has become appealing for understanding the computational principles of the nervous system by producing models based on biological evidence. In particular, networks that can assume a

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Real Time On-Chip Implementation of Dynamical Systems with Spiking Neurons WCCI 2012 IEEE World Congress on Computational Intelligence June, 10-15, 2012 - Brisbane, Australia IJCNN Real Time On-Chip Implementation of Dynamical Systems with Spiking Neurons Francesco Galluppi, Sergio Davies and Steve Furber

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Elon Musk to unveil brain chip with real-time neuron demonstration this week. Aug 25, 2020 | Featured, Science & Technology, Top Stories. Elon Musk 's brain-machine interface company, Neuralink, has an event scheduled for later this week to update the public on its progress since last year 's presentation. While the agenda is speculative for the most part, one expectation is a live demonstration of neuron activity.

Elon Musk to unveil brain chip with real-time neuron ...

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Real Time On-Chip Implementation of Dynamical Systems with Spiking Neurons Conference Paper (PDF Available) - June 2012 with 122 Reads How we measure 'reads'

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A real-time chip implementation for adaptive video coding control Abstract: The paper presents an adaptive coding control for real-time video coding systems. Based on temporal correlations, the group-of-pictures (GOP) of a video sequence is split into one basic GOP (BGOP) and many adaptive GOPs (AGOPs) and then processed accordingly.

A real-time chip implementation for adaptive video coding ...

Abstract: Single-pixel imaging (SPI) uses a single-pixel detector to create an image of an object. SPI relies on a computer to construct an image, thus increasing both the size and cost of SPI and limiting its application. We developed instant single-pixel imaging (ISPI), an on-chip SPI system that implements real-time imaging at a rate of 25 fps. ISPI uses the instant ghost imaging algorithm we proposed which leverages signal differences for image creation.

Instant single-pixel imaging: on-chip real-time ...

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The software Real Time Clock (RTC) is implemented using an 8-bit Timer/Counter with overflow interrupts enabled. Each timer overflow interrupt triggers an update of the software variables second, minute, hour, date, month, and year at the correct intervals. Figure 1-1. Oscillator Connection for Real Time Clock

AVR134: Real Time Clock (RTC) Using the Asynchronous Timer

The article presents the concept of real-time implementation computing tasks in video surveillance systems. A pipeline implementation of a multimodal background generation algorithm for colour video stream and a moving objects segmentation based on brightness, colour and textural information in reconfigurable resources of FPGA device is described.

[PDF] Real-Time Implementation of Moving Object Detection ...

If you need to run Linux or a real-time operation on a chip, the PolarFire SoC offers an unparalleled combination of thermal efficiency and defense-grade security to simplify the deployment of smart, connected systems. Deterministic, coherent 64-bit multi-core RISC-V CPU 25K to 460K Logical Elements (LEs) Up to 50% lower power than alternatives

System-on-Chip FPGAs | Microchip Technology

This paper deals with the real-time implementation of SPIHT algorithm using DSP chip. In order to facilitate the implementation and improve the codec's performance, some relative issues are thoroughly discussed, such as the optimization of program structure to speed up the wavelet decomposition.

Real-time implementation of a new low-memory SPIHT image ...

Real-time System Implementation for Video Processing. Paper ID #15811. Real-time System Implementation for Video Processing. Dr. Wagdy H Mahmoud, University of the District of Columbia Wagdy H. Mahmoud is an Associate Professor of electrical engineering at the Electrical Engineering Department at UDC. Mahmoud is actively involved in research in the areas of reconfigurable logic, hard- ware/software co-design of a system on a chip using reconfigurable logic, application-specific integrated ...

Real-time System Implementation for Video Processing

EMV is a payment method based upon a technical standard for smart payment cards and for payment terminals and automated teller machines which can accept them. EMV originally stood for "Europay, Mastercard, and Visa", the three companies which created the standard.EMV cards are smart cards, also called chip cards, integrated circuit cards, or IC cards which store their data on integrated ...

System-on-Chip for Real-Time Applications will be of interest to engineers, both in industry and academia, working in the area of SoC VLSI design and application. It will also be useful to graduate and undergraduate students in electrical and computer engineering and computer science. A selected set of papers from the 2nd International Workshop on Real-Time Applications were used to form the basis of this book. It is organized into the following chapters: -Introduction; -Design Reuse; -Modeling; -Architecture; -Design Techniques; -Memory; -Circuits; -Low Power; -Interconnect and Technology; -MEMS. System-on-Chip for Real-Time Applications contains many signal processing applications and will be of particular interest to those working in that community.

Computer scientists have long appreciated that the relationship between algorithms and architecture is crucial. Broadly speaking the more specialized the architecture is to a particular algorithm then the more efficient will be the computation. The penalty is that the architecture will become useless for computing anything other than that algorithm. This message holds for the algorithms used in real-time automatic control as much as any other field. These Proceedings will provide researchers in this field with a useful up-to-date reference source of recent developments.

This text provides a survey of the latest research into the Hough transform for line detection and its contemporary developments. Written with students in mind, this work can serve as a condensed textbook and as a reference for practitioners working in computer vision. The text also presents an overview and detailed elaboration of recent research related to PCLines—a line parameterization based on parallel coordinates. A detailed analysis of the concept is given, including implementation details and measurements. One chapter discusses the detection of chessboard-like patterns, and sets of parallel lines and lines coincident with one (vanishing) point—a topic with many applications, such as 2D barcodes, aerial images, and architecture recognition. The work summarizes recent research in the field, and analyses new advances achieved using the PCLines parameterization.

One of the most striking properties of biological systems is their ability to learn and adapt to ever changing environmental conditions, tasks and stimuli. It emerges from a number of different forms of plasticity, that change the properties of the computing substrate, mainly acting on the modification of the strength of synaptic connections that gate the flow of information across neurons. Plasticity is an essential ingredient for building artificial autonomous cognitive agents that can learn to reliably and meaningfully interact with the real world. For this reason, the neuromorphic community at large has put substantial effort in the design of different forms of plasticity and in putting them to practical use. These plasticity forms comprise, among others, Short Term Depression and Facilitation, Homeostasis, Spike Frequency Adaptation and diverse forms of Hebbian learning (e.g. Spike Timing Dependent Plasticity). This special research topic collects the most advanced developments in the design of the diverse forms of plasticity, from the single circuit to the system level, as well as their exploitation in the implementation of cognitive systems.

This book introduces a novel transcoding algorithm for real time video applications, designed to overcome inter-operability problems between MPEG-2 to H.264/AVC. The new algorithm achieves 92.8% reduction in the transcoding run time at a price of an acceptable Peak Signal-to-Noise Ratio (PSNR) degradation, enabling readers to use it for real time video applications. The algorithm described is evaluated through simulation and experimental results. In addition, the authors present a hardware implementation of the new algorithm using Field Programmable Gate Array (FPGA) and Application-specific standard products (ASIC). • Describes a novel transcoding algorithm for real time video applications, designed to overcome inter-operability problems between H.264/AVC to MPEG-2. • Implements algorithm presented using Field Programmable Gate Array (FPGA) and Application-specific Integrated Circuit (ASIC). • Demonstrates the solution to real problems, with verification through simulation and experimental results.

Chip Design and Implementation from a Practical Viewpoint Focusing on chip implementation, Low-Power NoC for High-Performance SoC Design provides practical knowledge and real examples of how to use network on chip (NoC) in the design of system on chip (SoC). It discusses many architectural and theoretical studies on NoCs, including design methodology, topology exploration, quality-of-service guarantee, low-power design, and implementation trials. The Steps to Implement NoC The book covers the full spectrum of the subject, from theory to actual chip design using NoC. Employing the Unified Modeling Language (UML) throughout, it presents complicated concepts, such as models of computation and communication—computation partitioning, in a manner accessible to laypeople. The authors provide guidelines on how to simplify complex networking theory to design a working chip. In addition, they explore the novel NoC techniques and implementations of the Basic On-Chip Network (BONE) project. Examples of real-time decisions, circuit-level design, systems, and chips give the material a real-world context. Low-Power NoC and Its Application to SoC Design Emphasizing the application of NoC to SoC design, this book shows how to build the complicated interconnections on SoC while keeping a low power consumption.

Hydroelectric power stations are a major source of electricity around the world; understanding their dynamics is crucial to achieving good performance. The electrical power generated is normally controlled by individual feedback loops on each unit. The reference input to the power loop is the grid frequency deviation from its set point, thus structuring an external frequency control loop. The book discusses practical and well-documented cases of modelling and controlling hydropower stations, focused on a pumped storage scheme based in Dinorwig, North Wales. These accounts are valuable to specialist control engineers who are working in this industry. In addition, the theoretical treatment of modern and classic controllers will be useful for graduate and final year undergraduate engineering students. This book reviews SISO and MIMO models, which cover the linear and nonlinear characteristics of pumped storage hydroelectric power stations. The most important dynamic features are discussed. The verification of these models by hardware in the loop simulation is described. To show how the performance of a pumped storage hydroelectric power station can be improved, classical and modern controllers are applied to simulated models of Dinorwig power plant, that include PID, Fuzzy approximation, Feed-Forward and Model Based Predictive Control with linear and hybrid prediction models.

The book constitutes the proceedings of the 23rd International Conference on Artificial Neural Networks, ICANN 2013, held in Sofia, Bulgaria, in September 2013. The 78 papers included in the proceedings were carefully reviewed and selected from 128 submissions. The focus of the papers is on following topics: neurofinance graphical network models, brain machine interfaces, evolutionary neural networks, neurodynamics, complex systems, neuroinformatics, neuroengineering, hybrid systems, computational biology, neural hardware, bioinspired embedded systems, and collective intelligence.

In the last 40 years, machine vision has evolved into a mature field embracing a wide range of applications including surveillance, automated inspection, robot assembly, vehicle guidance, traffic monitoring and control, signature verification, biometric measurement, and analysis of remotely sensed images. While researchers and industry specialists continue to document their work in this area, it has become increasingly difficult for professionals and graduate students to understand the essential theory and practicalities well enough to design their own algorithms and systems. This book directly addresses this need. As in earlier editions, E.R. Davies clearly and systematically presents the basic concepts of the field in highly accessible prose and images, covering essential elements of the theory while emphasizing algorithmic and practical design constraints. In this thoroughly updated edition, he divides the material into horizontal levels of a complete machine vision system. Application case studies demonstrate specific techniques and illustrate key constraints for designing real-world machine vision systems. - Includes solid, accessible coverage of 2-D and 3-D scene analysis. - Offers thorough treatment of the Hough Transform—a key technique for inspection and surveillance. - Brings vital topics and techniques together in an integrated system design approach. - Takes full account of the requirement for real-time processing in real applications.

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