

Digital Design With Rtl Design Vhdl And Verilog

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The emergence of parallel processing, multicore processors and FPGAs are blurring the lines between hardware and software and fundamentally altering the way digital design and design logic should be taught. Vahid's RTL-early approach better assists students in grasping the essential design fundamentals before digging into specific details of design optimization.

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5.4 More RTL Design 264. Additional Datapath Components for the Library 264. RTL Design Involving Register Files or Memories 265. RTL Design Pitfall Involving Storage Updates 271. RTL Design Involving a Timer 272. A Data-Dominated RTL Design Example 275. 5.5 Determining Clock Frequency 278. 5.6 Behavioral-Level Design: C to Gates (Optional) 281

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In digital circuit design, register-transfer level is a design abstraction which models a synchronous digital circuit in terms of the flow of digital signals between hardware registers, and the logical operations performed on those signals. Register-transfer-level abstraction is used in hardware description languages like Verilog and VHDL to create high-level representations of a circuit, from which lower-level representations and ultimately actual wiring can be derived. Design at the RTL level

[Register-transfer level - Wikipedia](#)

A student exposed to RTL design in a first course will have a more relevant view of the modern digital design field, leading not only to a better appreciation of modern computers and other digital devices, but to a more accurate understanding of careers involving digital design.

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RTL Design: The only major digital design book to emphasize RTL (register-transfer-level) design, central to the million-gate IC era, while continuing to introduce topics fully bottom-up. Teaches modern "Capture/Convert" top-down design methodology for combinational, sequential, and RTL design.

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Register Transfer Level (RTL) is an abstraction for defining the digital portions of a design. It is the principle abstraction used for defining electronic systems today and often serves as the golden model in the design and verification flow. The RTL design is usually captured using a hardware description language (HDL) such as Verilog or VHDL.

~~Register Transfer Level (RTL)—Semiconductor Engineering~~

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Logic design is a step in the standard design cycle in which the functional design of an electronic circuit is converted into the representation which captures logic operations, arithmetic operations, control flow, etc. A common output of this step is RTL description. Logic design is commonly followed by the circuit design step.

~~Logic synthesis—Wikipedia~~

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